Rapid Single Flux Quantum (RSFQ) – Design Rules

for Nb/Al_2O_3-Al/Nb-Process at

Version 22.06.2007

IPHT Jena

Address: **Institute of Photonic Technology (IPHT)**

Department of Quantum Detection
P.O. Box 100 239
D - 07702 Jena
Germany

Contact: Dr. H.-G. Meyer (Head of Department)

phone: + 49 3641 206116
FAX: + 49 3641 206198
e-mail: hans-georg.meyer@ipht-jena.de

Dr. J. Kunert (RSFQ Design)

phone: + 49 3641 206126
FAX: + 49 3641 206199
e-mail: juergen.kunert@ipht-jena.de

Internet: http://www.ipht-jena.de

RSFQ design rules IPHT Jena Version 1.2

Nb/Al_2O_3-Al/Nb-technology Process : RSFQ1D

Date: 6/22/2007

A. Photomasks:

Mask	GDSII No.	Name	Layout polarity	Color	Material	Thickness /nm	Description	Mask polarity	Wafer resist
A	1	M0	positive	yellow	Nb	200	Ground plane	dark	+
B	2	I0A	negative	magenta	Nb_2O_5	50	Holes in anodisation	clear	-
C	3	I0B	negative	magenta	SiO	200	Holes in isolation	clear	-
D	4	I0C			SiO		Reserved		
E	5	M1	positive	Red	Nb	250	Wiring1	dark	+
F	6	T1	positive	Cyan	Nb/Al/Nb	60/12/30	Trilayer package	clear	-
G	7	I1A	negative	Light blue	Nb_2O_5	70	Holes in anodisation, Definition of junction	clear	-
H	8	CUT	positive	Light gray	---	---	Cutting of bridges for anodisation	clear	+
I	9	I1B	negative	Light blue	SiO	150	Holes in isolation	clear	-
J	10	R1	positive	green	Mo	80	Resistance layer	clear	+
K	11	I2	negative	coral	SiO	150	Holes in isolation	clear	-
L	12	M2	positive	Blue	Nb	350	Wiring 2	dark	+
M	13	R2	positive	Dark green			Bond pads, optional	dark	-

Positive layout polarity means you design the physical structures as seen on the screen, negative means you design holes in the material. Clear mask polarity means that the mask is transparent wherever the patterns are drawn and dark means the opposite case.

B. Auxiliary Layers:

GDS II-No.	Name	Layout polarity	Place on mask	Description
15	SMA	Positive	all	Used for labels on masks
16	SMC	Positive	L-M2	Used for labels on chip
17	M0N	Negativ	A-M0	Defines holes in M0 plane by XOR with A-M0
18	TEXT	Positive	none	Used for help lines and notes
19	TERM	---	none	Defines ports for L-meter inductance calculation
20	INVERT	---	All with dark mask polarity	Area to invert polarity to use only masks with polarity clear

Remarks and auxiliary layers:

- Structures in layer SMA (GDS II-No. 15) are put **on all masks**.
- Holes in the M0 plane (moats) can be drawn on a separate layer M0N (GDS II-No. 17). For photo mask production this layer will be subtracted from layer M0 (GDS II-No. 1).
- TEXT layer (GDS II-No. 18) is used for additional text and other structures (lines, polygons etc.) during layout generation. It is **not put on masks**.
- To meet the correct value the holes in anodisation will be increased of 100nm by a resize operation during data prepatation

C. Basic design rules:

1. Patterns (for all layers)

- Only polygon patterns with edge angles of 45°, 90° and 135° should be used.

For example :

(an customer has to take in account that using of an edges with angles different from n×45° are approximated with rectangular steps).

- Data points on a grid smaller than 0.1 µm will be rounded to this 0.1 µm during compilation of the data for the e-beam writer.
- The number of edges should be as low as possible. That means that one big

Rectangle is better than such a structure (if it is possible).

It is recommended
to use a grid of 2.5 µm for the corners of polygons and the centers of Josephson junctions (JJs). Only in special cases other grid values should be used. It is strongly recommended to use a grid of 25 µm for long interconnection lines. This means, that at least one edge of patterns in M2, M1 or M0, which have to be connected to the contact pads, must be on the 25 µm grid.

2. Width and spacing inside single layers

2.1 Layers M0, M1, M2:

- Width ≥ 5 µm.
- Spacing ≥ 5 µm, ≥ 2.5 µm if strip length ≤ 75 µm.

2.2 Layer M2:

- Width W and spacing S of long interconnection lines between circuits and contact pads should be as large as the layout permits (standard value W = S, W = 100 µm).

2.3 Layer I0A, I0B, I1A, I1B, I2:

- Minimum contact hole size is 5 µm × 5 µm,
- Spacing between different contact holes is ≥ 5 µm.
- Spacing Inside I0A, I1A ≥ 2.5 µm

2.4 Layer I1A:

- Size of Josephson junction is defined by I1A. The JJs have a octagon form and the smallest JJ has an area of 12.5 μm^2 with an inner diameter (see page 7) of the octagon of 3.8 µm.

2.5 Layer CUT:

- For cutting wires in M0 or M1; these lines have to be longer than 15 µm.

2.6 Layer T1:

- Spacing $\geq$ 5 µm.
- T1 used only to form JJ. Size of JJ is defined by I1A.

2.7 Layer R1:

- Width $\geq$ 5 µm.
- Spacing $\geq$ 5 µm, $\geq$ 2.5 µm if strip length $\leq$ 75 µm.
- Widths of bias resistors are fixed to 10 µm, spacing $\geq$ 5 µm.
- Widths of shunt resistors should be no less than 10 µm, spacing $\geq$ 5 µm.

3. Spacing between different layers

3.1 All layers:

- Spacing between edges of structures in different layers is usually $\geq$ 2.5 µm.
- Exception in JJ: If area of I1A < area of I2A then distance > 2.0 µm.

3.2 Layers T1, I1B, and I2:

- Radius of octagonal area in T1 for JJs is 2.0 µm larger than the radius of window in isolation layer I1B. T1 and I2 coincide.

3.3 Layers T1 and M1:

- Distance to next edges below has to be $\geq$ 2.5 µm.

3.4 Layers I1A and I1B:

- Radius of octagonal contact holes in I1B for JJs is 2.0 µm larger than the radius of JJs (I1A).
- For vias: spacing between I1B and I1A is $\geq$ 2.5 µm.

3.5 Layers I1B and I2:

- Radius of octagonal contact holes in I2 for JJs is 2.0 µm larger than the radius of holes in I1B.
- For vias: spacing between I1B and I2 is $\geq$ 2.5 µm.

3.6 Layers I1A and I2:

- Edges of contact holes in I1A may coincide with I2, if smallest size in via is defined by I1B.

3.7 Layers CUT, I0A, I0B, and I1A:

- Below CUT edges of I0A, I0B and I1A may coincide.
- If CUT, I0A, I0B, and I1A coincide, then CUT can cross structures in M0 or M1, but not both.

- Spacing Between I0A and I1A ≥ 2.5 µm

3.8 Layers CUT, and T1:

- Spacing between CUT and T1 is ≥ 19 µm.

3.9 Layers M2, and I1A:

- Radius of octagonal area in M2 for JJs is 2.5 µm larger than the radius of window in isolation layer I1A.

4. Overlap and crossing of edges between different layers

4.1 Vias:

- Overlap distance for metallisation to largest window in isolation/anodisation is 2.5 µm.
- Via from M0 to M2 must include M1.

4.2 Layer T1:

- Crossing of any structure by T1 is not allowed.

4.3 Layer R1:

- It is only possible to connect R1 by M2 using holes in I2. Other crossings of any structure by R1 are not allowed.
- Distance to next edges below has to be ≥ 2.5 µm.

4.4 Layers R1 and I2:

- Outside the connection with M2 the R1 has to be covered by I2.

4.5 Layers R1 and M2:

- In the contact hole of layer I2 the resistor has to be covered completely by M2. Overlap of M2 and R1 in the windows of I2 has to be 2.5 µm for shunting resistors and 5 µm for the bias current resistors.
- Crossings of R1 and M2 should be avoided as far as possible.

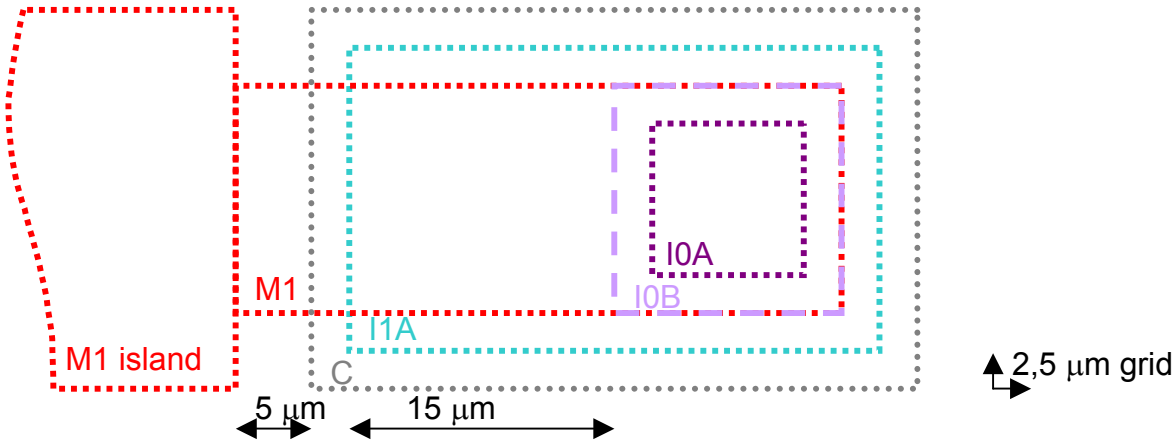
We offers Design Rules Check (DRC) for customers. The layouts will be checked before starting photo mask preparation.

5. Chip placement on wafer

The wafer size is 4 inch in diameter. One wafer contains 32 chips placed in the center, structures for photo mask alignment and a contact pad for the anodisation. The chip size is 12.8×12.8 mm^2 with user area of 12.7×12.7 mm^2, cf. appendix 3. The distance of 0.1 mm between different chips is necessary for cutting of the chips. For anodisation each chip has to be connected to a 100 µm wide wire between the chips. This has to be done in layer M0.
Our standard chip contains 48 contact pads each with a size of 0.65×0.65 mm^2 and placed on chip edges on a 50 µm distance from the border the of chip. The distance between the centers of the contact pads is 1.005 mm.
Customers can realize their own chip dimensions. If wanted, customers can use library cells (JJs of different dimensions, shunted JJs, sections of Josephson Transmission Lines, chip outline, pads, ...).

6. Anodisation and cutting

Anodisation of the surface of Niobium is necessary for a good isolation between the metal layers. Therefore all structures in M0 have to be connected to the 50 µm wide wire around the chip. If this is not guaranteed by layout, this has to be done with additional wires. Later these additional wires have to be removed. The same has to be done for M1. In M1 it is also possible to make connections to M0. The additional wires for anodisation are removed by the cutting process step. To cut wires it is necessary to put a window for anodisation and isolation below the cut frame. That means for removing a bridge in M1 you have to put windows in I1A and CUT, for removing a bridge in M0 you have to put windows in I0A, I0B, I1A and CUT. The overlap of M0 or M1 and CUT must be more than 15 µm. The length of metal path between design structure and CUT window edge must be more than 5 µm. For anodisation M1 islands we recommend following structure.



Recommended design of a cut able contact structure for anodisation of M1

7. Requirements for GDS II file correctness

- GDS II files must be in BLOCK FORMAT, i.e. in size portions of 512 bytes (mostly by default),
- For POLYGONS (GDS II : BOUNDARIES) you can not use non-orientable self-intersecting polygons. Only orientable self-intersecting polygons (also called re-entrant boundaries) are allowed,
- DATATYPES are ignored,
- Zero width PATHS and TEXT can be used for documentation in layer TEXT,
- For physical text on the mask/wafer you can not use POLYGONS or PATHS, only GDS II TEXT in layer SMC (GDS II-No. 16). You can use font0, font1, font2, and font3 (without font names),
- TEXT will be represented on the mask/wafer by a simple rectangular font,
- Use only PATHTYPE 0 (normal) or 2 (extended), not PATHTYPE 1 (rounded),
- USER UNIT = 1x10E-6,
- RESOLUTION = 0.001 user unit.

D. Technology description:

1. Josephson junctions parameters

	Nominal value	Intra wafer tolerance	On wafer homogeneity	On chip homogeneity
Josephson current density	1000 A/cm^2	± 20 %	± 15 %	≤ ± 5 %
Sheet resistance of Mo-layer	1.0 Ω	± 20 %	± 10 %	≤ ± 5 %

2. Stripline inductance

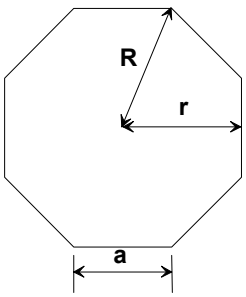
Layer	L_{square}	Intra wafer tolerance	On wafer homogeneity	On chip homogeneity
M1-M0	0.52 pH	± 10 %	± 5 %	≤ ± 2 %
M2-M1 (across M0)	0.64 pH	± 10 %	± 5 %	≤ ± 2 %
M2-M0	0.81 pH	± 10 %	± 6 %	≤ ± 2 %

Remarks:

- **Inductances** were measured in interferometers with micro strips of 100 µm length and 10 µm width.
- **London penetration depth** for magnetic field: (87 ± 5) nm.
- **Capacitance:** Measured value of specific capacitance (defined from Fiske steps; measurements at JJs with w = 10 µm l = 30 µm and 100 µm) is (0.05 ± 0.002)pF/µm^2.

3. Nominal values of area, critical current, diameter, and shunt resistor for JJs

A/µm^2	12.5	17.7	20.6	23.8	30.8	36.7	59.9
I_c/units*	1.00	1.50	1.75	2.00	2.50	3.00	5.00
I_c/µA	125	187.50	218.75	250	312.50	175	625.00
∅/µm	3.8	4.6	5.0	5.4	6.1	6.7	8.5
C_J/pF	0.625	0.885	1.03	1.19	1.54	1.835	3.0
R_s/Ω**	2.10	1.40	1.20	1.05	.85	.70	.40



∅ = 2r

Remarks:

*The normalized I_c values are for developers using PSCAN. The unit I_c is 125 µA.

**The R_s value is calculated for adjusting β_c=1.

- JJs areas are realized as octagons.
- Measured ratios of critical currents are correct within ± 5 %.
- The nominal I_cR_n value is about 256µV.

E. Multi custom wafer rules:

To reduce costs we recommend to place designs of some customers together on one wafer. For decreasing the time of placement and better matching conditions:

- Send flat hierarchy designs including only the top cell
- Use chip size of 12.8mm x 12.8 mm, 6.4mm x 6.4mm or 5mm x 5mm
- Set the origin [point 0, 0] to the lower left corner and follow gds2 design rule [rule 7]

F. Future plans for improvement of the Niobium process:

At this time the development of our technology is still in progress. Therefore in the next release of our technology description some changes will be made.

G. Note:

Violation of the design rules may be permitted in special cases, e.g. for connections between trilayer and wiring.

H. Release Notes:

Version 1.1, Date 24.8.2005:

3.8 Layers CUT, and T1:

- Spacing between CUT and T1 is ≥ 19 µm.

3.9 Layers M2, and I1A:

- Radius of octagonal area in M2 for JJs is 2.5 µm larger than the radius of window in isolation layer I1A.

Version 1.2, Date 22.06.2007

A. Photomaske: Column "Wafer resist"

2.3 Layer I0A, I0B, I1A, I1B, I2:

- Spacing Inside I0A, I1A ≥ 2.5 µm

3.7 Layers CUT, I0A, I0B, and I1A:

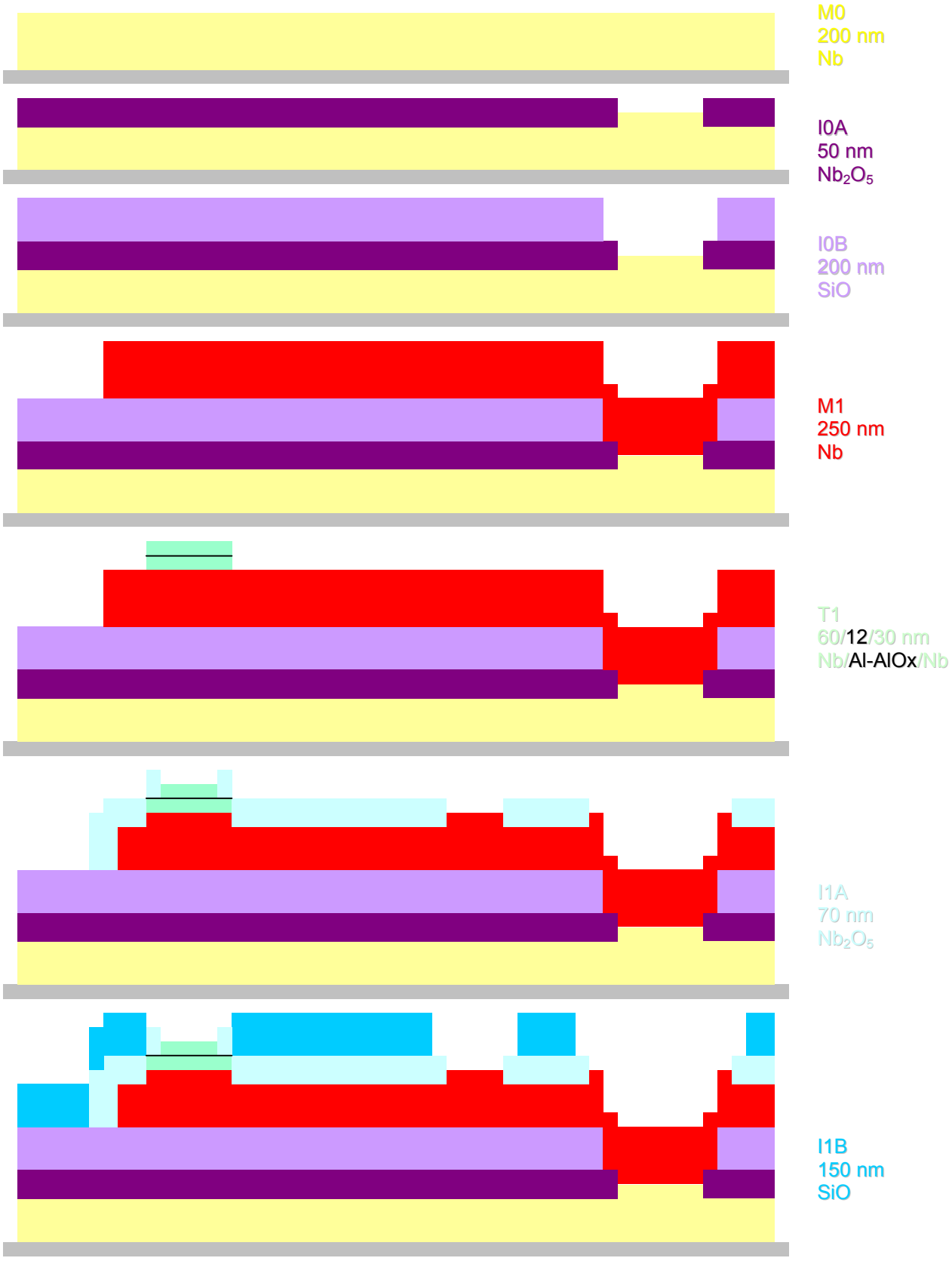
- Spacing Between I0A and I1A ≥ 2.5 µm

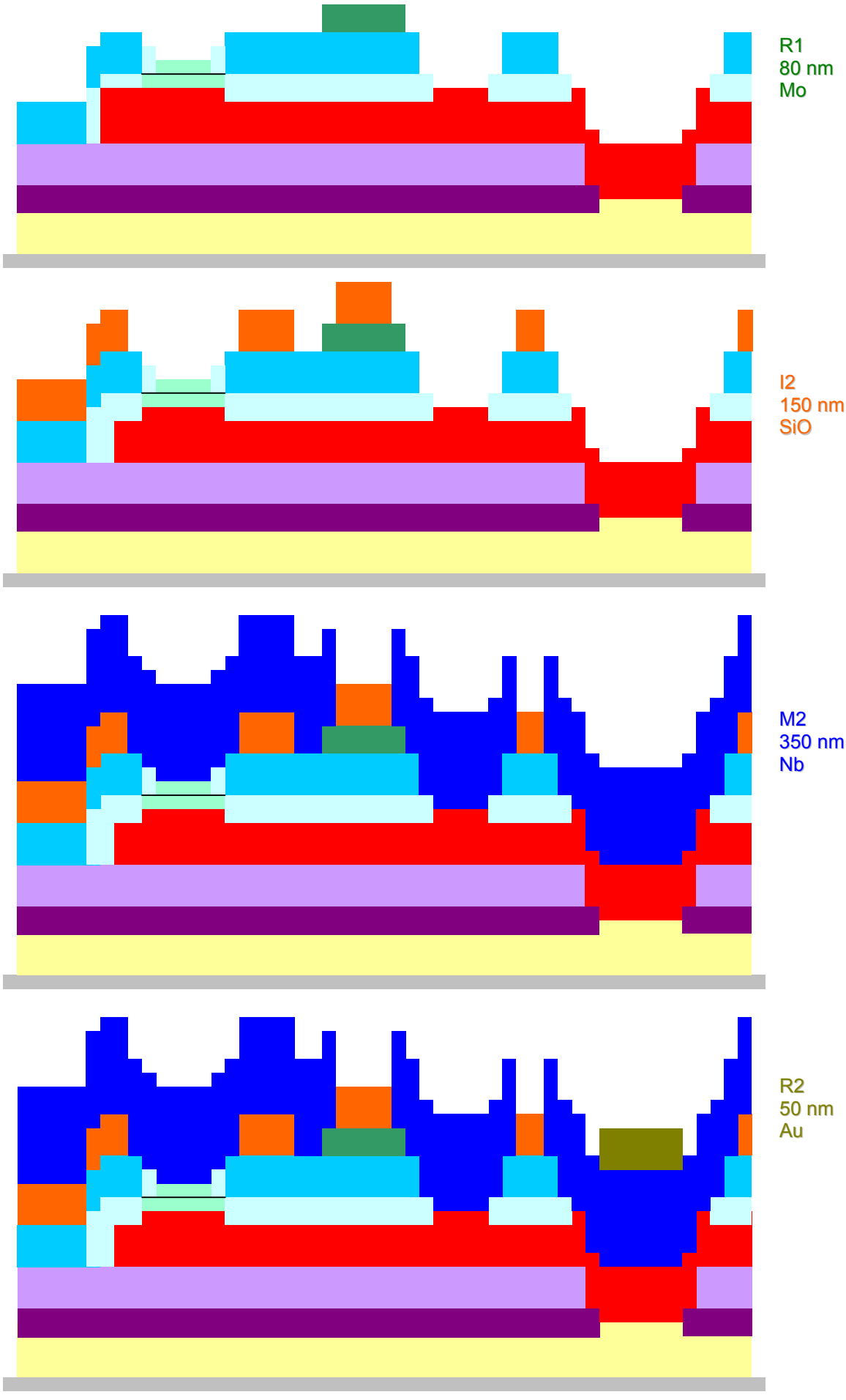
I. Appendix:

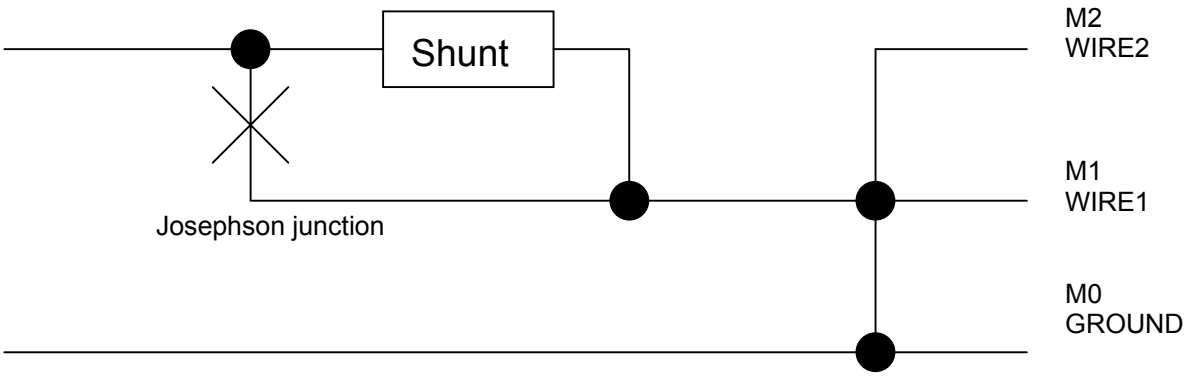
1. Contents of the FLUXONICS Foundry layout library

- Josephson Junctions, shunted and unshunted,
- Pads,
- Chip outline,
- Vias,
- Resistors,
- dc/SFQ & SFQ/dc (dc to Single Flux Quantum & Single Flux Quantum to dc) converters.

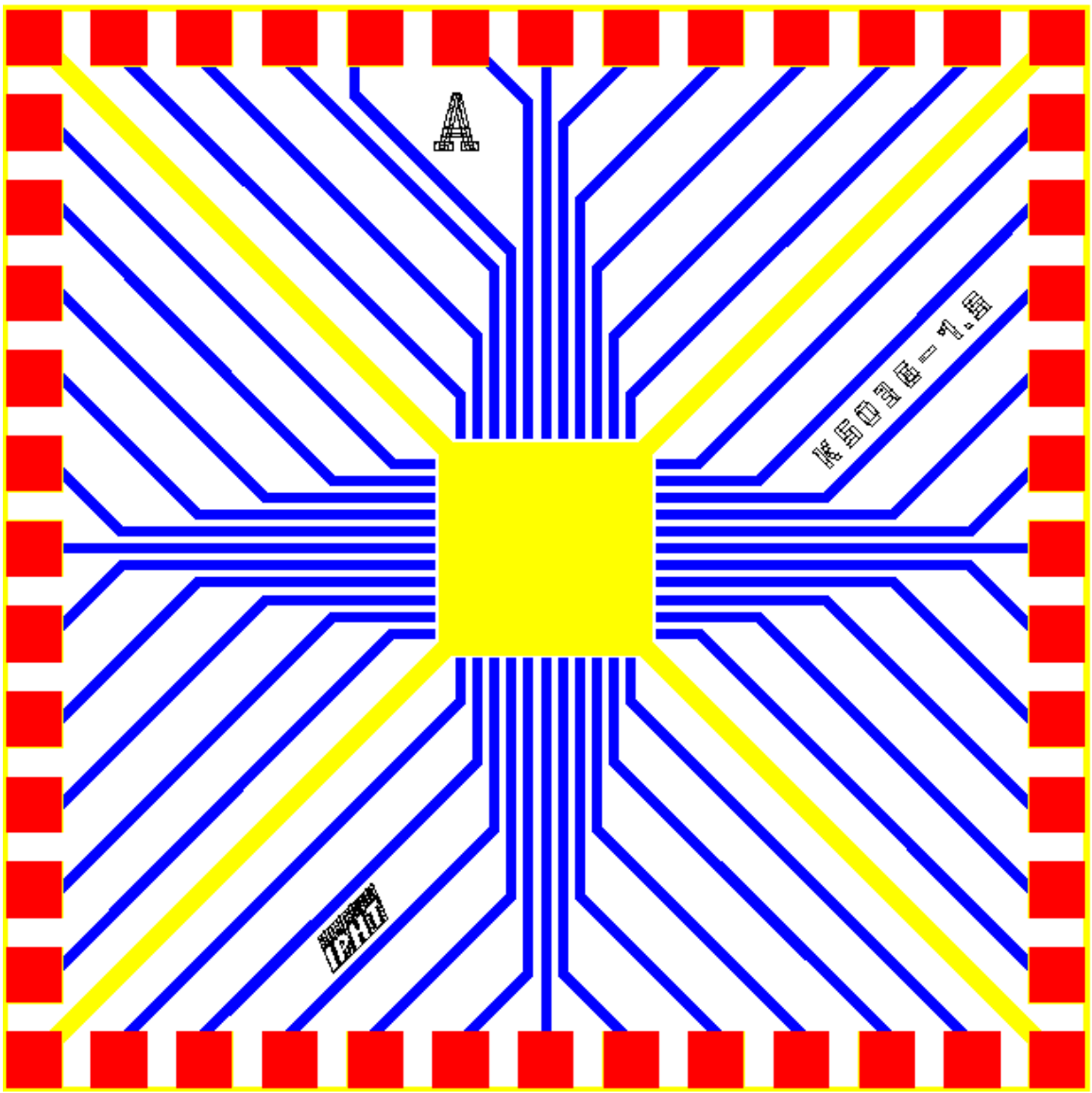
2. Cross section of RSFQ sandwich for the process RSFQ1D




R1
80 nm
Mo
I2
150 nm
SiO
M2
350 nm
Nb
R2
50 nm
Au



3. Standard RSFQ chip layout



The standard chip layout: dimensions 12.8 × 12.8 mm^2, 48 contact pads with dimensions 0.65 × 0.65 mm^2 each.